Preliminary - NDA Required

SEAforth® 40C18

Scalable Embedded Array™ Processor

FEATURES

- Forty C18 core processors capable of up to 25 billion operations per second
- Fully asynchronous for fast processing, low power
- External memory interface
- SPI, serial, and parallel ports
- 2 SERDES ~400 Mbit
- Three 18-bit A/D converters
- Three 9-bit D/A converters
- Zero-overhead inter-processor communication and synchronization

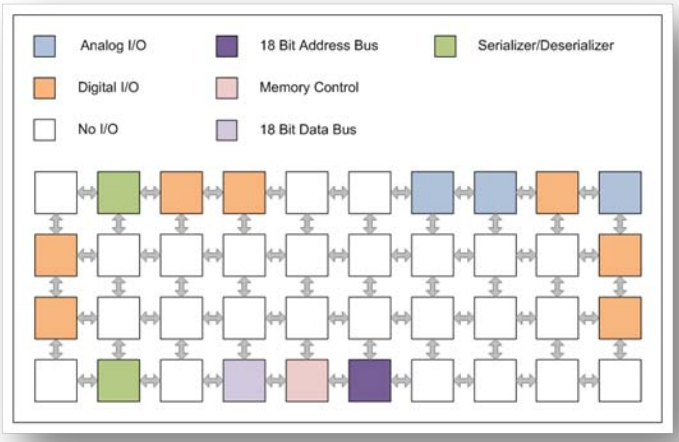
TARGET APPLICATIONS

- Consumer audio processing
- Wireless devices
- Home automation
- Remote data collection and processing
- Security applications
- Battery powered portable medical devices
- Industrial control and instrumentation
- Automotive control
- Sound processing

OVERVIEW

The SEAforth 40C18 is one of the IntellaSys® Scalable Embedded Array multicore processors. It has an array of 40 cores; each of the C18 cores is a complete computer, with its own ROM, RAM, and interprocessor communication. Together they can deliver up to 26 billion operations per second. The SEAforth 40C18 is a perfect embedded computer solution for consumer applications that demand high processing power and low power dissipation.

With 40 nodes to work with, designers can dedicate groups of them to specific tasks such as FFT and DFT algorithms. The result is a tightly coupled, extremely versatile user-defined group of dedicated processors assigned to specific tasks. Some can be doing highly compute-intensive audio processing, while others handle wireless interfaces, external memory, and user interface functions. And since each core has its own ROM and RAM, there is less need to go to external memory.



BLOCK DIAGRAM – SEAforth 40C18

Each core runs asynchronously, at the full native speed of the silicon. During interprocessor communication, synchronization happens automatically; the programmer doesn't have to create synchronization methods. Communication happens between neighbors through dedicated ports. A core waiting for data from a neighbor goes to sleep, dissipating less than one microwatt. Likewise, a core sending data to a neighbor not ready to receive it goes to sleep until that neighbor accepts it.

A wake up occurs instantly upon the rising edge of the synchronizing signal. With the wake up logic controlling power use, there is no need for complex power control strategies. Power is conserved as a natural consequence of good program design. External I/O signals may also be used to wake up sleeping processors. The small size and low power make the SEAforth 40C18 a good value both in terms of MIPS per dollar and MIPS per milliwatt.

I/O ports on the SEAforth 40C18 are highly configurable because they are controlled by firmware. The 4-wire SPI port, the 2-wire serial ports, and the single-bit GPIO ports can be programmed to perform a large variety of functions. With the available processing power, wireless solutions become possible without the need for separate wireless chips. Ports can be programmed to support I2C, I2S, asynchronous serial, or synchronous serial ports. Serial ports can also be used to connect multiple SEAforth S40C18s.

In addition to serial I/O, two nodes have dedicated parallel I/O ports. These can be used for parallel I/O, or when combined, can drive an external memory device.

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THE C18 CORE

Each C18 core in a SEAforth device is identical to the others in terms of opcodes and architecture. Individual cores have different I/O options, and the ROM-based firmware differs slightly as well. Each core is a 18-bit computer that is a Forth stack machine. Its instruction set consists of 32 basic opcodes. It uses a data stack for parameters and a return stack for control flow.

- 18-bit stack oriented computer
- Runs VentureForth language as native code
- Executes one ALU operations per 1.5 ns
- Zero –overhead interprocessor communication and synchronization
- 64 words RAM / 64 words ROM
- < 3.5 mA per core at full speed
- Automatic sleep mode at < 5 mA per core

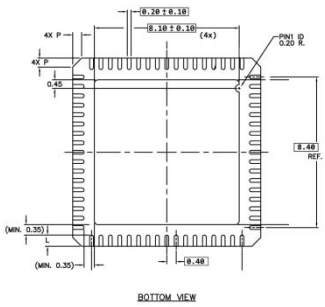
VENTUREFORTH®

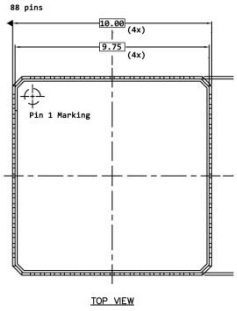
VentureForth programming language is the native machine code for the SEAforth processors. As a RISC version of the well established Forth software language , VentureForth provides 32 powerful instructions including a full 18x18 bit hardware-based multiply step and micro FOR/NEXT loops for reading, sending blocks of data.

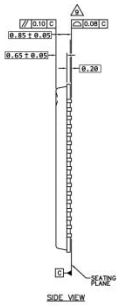
VentureForth programming frees designers from laboring over thousands of lines of assembly code. Moreover, it creates extremely compact code that is quick to write and debug. User code is compiled for each processor's RAM and at boot time, code is stream loaded into each core processor's RAM. It is VentureForth that enables SEAforth processors to be easily scalable.

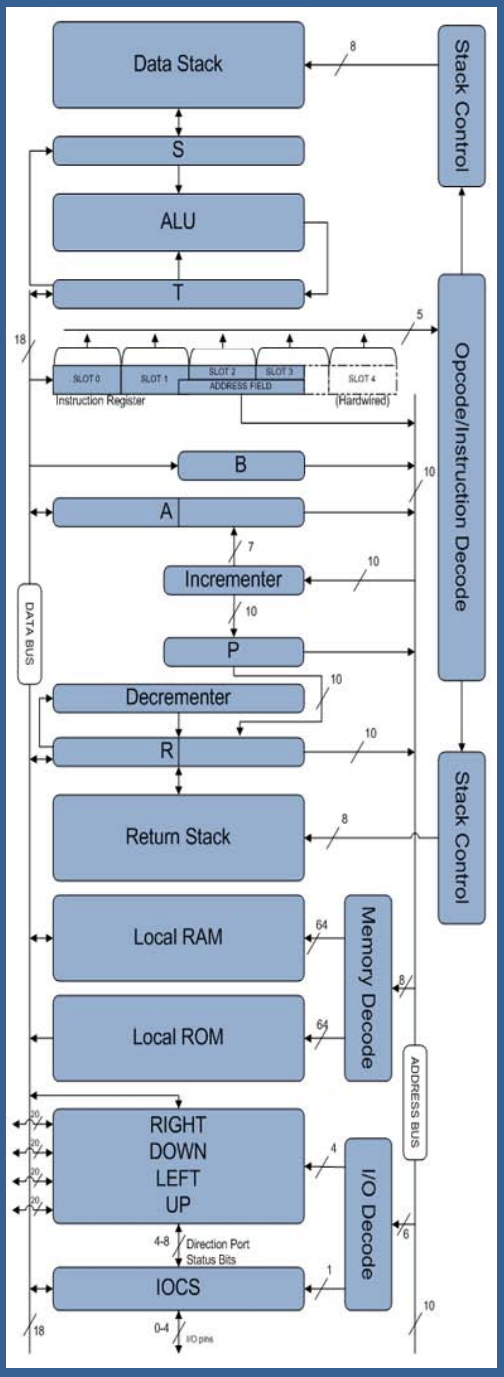
PACKAGE

The SEAforth 40C18 is packaged in a 10 x 10 mm 88-pin QFN.









THE C18 CORE

intellaSys
inventive to the core

For more information, visit **www.intellasys.net**

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